I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2001-016302 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FEB. 21. 2006

Tadahiko ITOH
Patent Attorney
ITOH International Patent Office
32nd Floor,
Yebisu Garden Place Tower,
20-3 Ebisu 4-Chome, Shibuya-Ku,
Tokyo 150-6032, Japan

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This is to certify that the annexed is a true copy of the following application as filed with this office.

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Commissioner,
Patent Office Kouzo Oikawa (Seal)

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(Inventor)	
(Residence or Address)	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan
(Name)	Haruo SHOJI
(Applicant for Patent)	
(Identification Number)	000005223
(Name)	FUJITSU LIMITED
(Attorney)	
(Identification Number)	100070150
(Residence or Address)	32nd Floor, Yebisu Garden Place Tower 20-3, Ebisu 4-chome, Shibuya-ku Tokyo, Japan
(Patent Attorney)	
(Name)	Tadahiko Itoh
(Telephone Number)	03-5424-2511
(Indication of Official Fees)	
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[Name of the Document] Specification

[Title of the Invention]

A SEMICONDUCTOR MEMORY DEVICE, A SECTOR-ADDRESS CONVERSION CIRCUIT, AN ADDRESS-CONVERSION METHOD, AND OPERATION METHOD OF THE SEMICONDUCTOR MEMORY DEVICE

[Claims]

[Claim 1]

A semiconductor memory device, comprising a plurality of areas, each accommodating one or more small sectors in a predetermined physical address of each area, or in a series of a plurality of physical addresses including the predetermined physical address of the area, said predetermined physical address being one of a highest physical address of the area.

[Claim 2]

A semiconductor memory device, comprising a plurality of areas, each accommodating one or more small sectors in a predetermined physical address of each area, or in a series of a plurality of physical addresses including the predetermined physical address of the area, said predetermined physical address being one of a lowest physical address of the area.

[Claim 3]

The semiconductor memory device as claimed in any one of claims 1 and 2, comprising:

a plurality of sectors larger than one or more of the small sectors in each of the plurality of the areas; and

an address-conversion circuit configured to perform conversion of a sector address inputted from an

outside source to make the plurality of the areas function as the same boot block type.

[Claim 4]

The semiconductor memory device as claimed in claim 3, wherein the address-conversion circuit controls conversion of the sector address based on a signal specifying a boot block type, inputted from the outside source.

[Claim 5]

The semiconductor memory device as claimed in claim 3, wherein the address-conversion circuit is a control circuit for controlling the semiconductor memory device, which controls conversion of the sector address based on an inputted command specifying a boot block type.

[Claim 6]

The semiconductor memory device as claimed in any one of claims 1 through 5, which is capable of storing one of a rewriting program and a boot program into one or more of the small sectors at any time.

[Claim 7]

An address-conversion method that enables a plurality of areas, each having a plurality of sectors, of a semiconductor memory device to function as the same boot block type, comprising:

converting a sector-address inputted from an outside source by a sector-address conversion circuit; and

connecting the sector-address conversion circuit to the semiconductor memory device having the plurality of areas, each having a plurality of sectors.

[Claim 8]

A sector-address conversion circuit that enables a memory device having a plurality of sectors to function as a desired boot block type, comprising:

a sector-address input terminal;

a sector-address output terminal;

a boot block type specifying terminal that specifies a desired boot block type of the memory device; and

a signal conversion circuit that converts a sector address inputted to the sector-address input terminal based on a signal inputted to the boot block type specifying terminal and a most significant bit of the sector address, and outputs a converted sector address from the sector-address output terminal.

[Claim 9]

The sector-address conversion circuit as claimed in claim 8, further comprising a control circuit for controlling the semiconductor memory device, which specifies a boot block type by providing a command.

[Claim 10]

An operation method of operating the semiconductor memory device claimed in any one of claims 1 through 6, said semiconductor memory device being split into two areas, each having one or more small sectors, comprising:

loading a rewriting program to one or more of the small sectors of a first area;

rewriting a uniform sector of a second area using said rewriting program stored in the first area;

loading a rewriting program to one or more of the small sectors of the second area; and

rewriting a uniform sector of the first area using

said rewriting program stored in the second area.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention relates to a semiconductor memory device, a sector-address conversion circuit, an address-conversion method, and an operation method of the semiconductor memory device.

[0002]

[Prior Art]

Various kinds of memory devices including a flash memory are known. Generally, the first operation at starting of a system, reset operation and the like is performed by reading a read-only boot program and the like from a memory device.

[0003]

Conventionally, a boot block used as an object for starting of a system occupies a small sector in a memory device, and is located in the high end or the low end of sector addresses (physical addresses) of the memory device (a bottom boot type or a top boot type, respectively, and called a boot block type) according to a requirement specification of the system. The two types are marketed as distinctly individual products.

[0004]

Fig.1A shows the top boot type memory device wherein a small sector 11 located at the highest sector addresses of the memory device serves as the boot block area.

[0005]

Fig. 1B shows the bottom boot type memory device wherein a small sector 16 located at the lowest sector addresses of the memory device serves as the boot block area.

[0006]

For an STB (set top box), there is a need to write new data while keeping data in a memory currently used in the system. That is, when there is an option service newly added and the like, it is necessary to write data or a program transmitted from a circuit to the memory device, while watching television through a television circuit.

[0007]

The STB has two memory devices 20 and 25 as shown in Fig.2. The memory device 20 is rewritten using a program stored in a boot block area 26, keeping data in the memory device 25. Further, the memory device 25 is similarly rewritten using a program stored in a boot block area 21, keeping data of the memory device 20. Thus, two memory devices are used to rewrite contents of the other memory device alternately.

[0008]

Moreover, as shown in Fig.3, a memory device that has small sectors 31 and 32 in the sectors of the highest addresses and the lowest addresses, respectively, is also available.

[0009]

In addition, the boot program is stored in the lowest physical addresses of a memory device when the small sector is located in the lowest addresses of the memory device.

Moreover, the boot program is stored in the highest physical addresses of a memory device when the small sector is located in the highest addresses of the memory device.

[0010]

[Problems to be Solved by the Invention]

However, rewriting of the data within the same system and the like always requires to use the same boot block type from design restrictions, and rewriting between memory devices with different boot block types has a problem that it cannot be easily performed.

[0011]

Moreover, a type of a memory device that has two or more banks, each having a small sector that can be used as a boot block, and rewriting each other is also marketed.

[0012]

However, a problem with this type is that address areas of the boot block differ (e.g. a bank or some banks are the top boot block type and the other banks are the bottom boot block type), causing difficulties in rewriting the memory device.

[0013]

The present invention aims at providing a semiconductor memory device that can be operational in a desired boot block mode, regardless of the original boot block type of the device, by facilitating rewriting of the memory device.

[0014]

[Means to Solve the Problems]

In order to provide the above-mentioned subject, the present invention adopts means as described hereunder.

[0015]

According to an aspect of the present invention, a semiconductor memory device (for example, a flash memory) is split into a plurality of areas (for example, banks) wherein the plurality of the areas accommodate a plurality of small sectors (for example, as shown in Fig. 5C) in the highest physical address in the areas or in a series of a plurality of the physical addresses containing the highest physical address in the areas.

[0016]

According to an aspect of the present invention, a semiconductor memory device is split into a plurality of areas wherein the plurality of the areas accommodate a plurality of small sectors (for example, as shown in Fig. 5A) in the lowest physical address in the areas or in a series of a plurality of the physical addresses containing the lowest physical address in the areas.

[0017]

The present invention enables easy rewriting of a memory while maintaining contents of another memory by splitting a semiconductor memory device into a plurality of areas wherein the plurality of the areas accommodate a plurality of small sectors in the highest or the lowest physical address.

[0018]

According to an aspect of the present invention, the semiconductor memory device includes a plurality of

sectors larger than one or more of the small sectors in each of the plurality of the areas and an address-conversion circuit (for example, Figs. 8, 9 and 10) configured to perform conversion of a sector address inputted from an outside source to make the plurality of the areas function as the same boot block type.

[0019]

The present invention further enables conversion of a boot block type of a semiconductor memory device that has a plurality of areas wherein a plurality of the small sectors are provided in addition to a plurality of sectors larger than the small sectors regardless of the boot block type of the semiconductor memory device.

[0020]

According to an aspect of the present invention, in the semiconductor memory device, the address-conversion circuit controls conversion of the sector address based on a signal (for example, bottom signal or top signal as shown in Fig. 8A) specifying a boot block type, inputted from the outside source.

[0021]

According to an aspect of the present invention, in the semiconductor memory device, the address-conversion circuit is a control circuit for controlling the semiconductor memory device, which controls conversion of the sector address based on an inputted command (for example, "AAH", "55H", and "2FH" shown in Fig. 11) specifying a boot block type.

[0022]

According to the above description, in the semiconductor memory device, the address-conversion circuit is specified.

[0023]

Accordingly, with a simple structure, sector address can be converted.

[0024]

According to an aspect of the present invention, the semiconductor memory device is capable of storing one of a rewriting program and a boot program into one or more of the small sectors at any time.

[0025]

According to the above description, the program stored in the small sectors is prescribed.

[0026]

The present invention provides a semiconductor memory device that can be used at the time of starting a system (at a power up, a rebooting, a resetting and the like) and rewriting by storing a rewriting program or a boot program in the small sector in the semiconductor memory device at any time.

[0027]

The address conversion circuit is applicable to a semiconductor memory device having a plurality of sectors, each of which further has a plurality of sectors. Thereby, the sector address inputted from the outside is converted by the address conversion circuit connected to the address conversion circuit such that the plurality of the areas

operate as the same boot block type.

[0028]

According to the above description, the method is applicable to the above described semiconductor memory device.

[0029]

The present invention also provides a sector-address conversion circuit that includes sector-address input terminals (for example, 100 through 103 shown in Fig. 8A), sector-address output terminals (for example, 110 through 113 shown in Fig. 8A), boot block type specifying terminals (for example, 104 and 105 as shown in Fig. 8A) to specify the boot block type of a memory device and sector-address conversion circuits (for example, 70 through 77 as shown in Fig. 8A) with a signal conversion circuit. The above-mentioned signal conversion circuit converts a sector address impressed to the sector-address input terminals, based on the most significant bit (for example, A19) and a signal impressed to the above-mentioned boot block type specifying terminals. The above-mentioned sector-address conversion circuit makes the memory device including the above-mentioned sectors to operate as a desired boot block type by outputting the sector-address converted by the above-mentioned signal conversion circuit from the sector-address output terminals.

[0030]

The above-mentioned sector-address conversion circuit can be a control circuit of the semiconductor memory device, which may be structured such that a boot block type specifying command can be inputted.

[0031]

The above described sector-address conversion circuit is applicable to the above described semiconductor memory device.

[0032]

The present invention provides a method to use the semiconductor memory device having two areas. That is, a rewriting program is loaded to a small sector of one of the two areas (for example, step S11 shown in Fig. 12), called the first area that rewrites a uniform sector of the other area (for example, step S12 shown in Fig. 12), called the second area, then the rewriting program is loaded to the small sector of the second area (for example, step S15 shown in Fig. 12) to rewrite the uniform sector of the first area (for example, step S16 shown in Fig. 12).

[0033]

The above described method is applicable to the above described semiconductor memory device having two areas.

[0034]

[Embodiments of the Invention]

In the following, an embodiment of the present invention is described with reference to the accompanying drawings.

[0035]

First, the principle of the sector address conversion of the memory device of this invention will be described with reference to Figs.4A, 4B and 4C and Fig.5.

[0036]

As shown in Fig.4A, a sector address from the outside is inputted into a sector-address conversion circuit 40. By the sector-address conversion circuit 40, the address is converted into a sector address of the internal address, and a memory cell array (memory device) is accessed through an address decoder circuit 41.

[0037]

The memory device can be accessed from the outside as a top boot type or a bottom boot type memory device as required by the sector-address conversion circuit 40, regardless of whether the memory device is (originally) a top boot type or a bottom boot type.

[0038]

The memory device shown in Fig.4B has two banks 48 and 49, each of which includes a uniform sector 42 and a small sector 43. Since the lower part of the drawing represents LSB (Least Significant Bit) and the upper part represents MSB (Most Significant Bit), each bank is structured as a bottom boot type.

[0039]

Then, if the sector of the memory device is accessed in the order of physical addresses as shown by arrows 44 and 45, without using an address decoder circuit 41 (or without changing the address if the address decoder circuit 41 is used) , the two banks 48 and 49 function as bottom boot type banks.

[0040]

However, if the sector-address conversion

circuit 40 changes the sector address such that it appears to the outside that the address is set up in the order as shown by arrows 46 and 47, the two banks 48 and 49 function as top boot type banks.

[0041]

Thus, the present invention enables a memory device with a plurality of small sectors to function as a plurality of devices with a top boot type or bottom boot type by preparing the address-conversion circuit that defines a boot block area in one of the upper or the lower areas of the sector address of the memory device.

[0042]

Fig.5A describes a memory device with three units of the bottom boot type bank that is shown in Fig.4B, and Fig.5C describes a memory device with three top boot type banks. Here, although the embodiment is described around a memory device with two or three banks, the number of banks in the present invention is not limited to two or three, but the invention can apply to a memory device with any plurality of banks.

[0043]

Fig.5B shows a case where the memory device of Fig.3 is divided into two banks. If viewed from a physical address, a bank 53 is a bottom boot type and a bank 54 is a top boot type. In contrast thereto, if the address is made to appear to the outside in the order as shown by arrows 55 and 56 by using the sector-address conversion circuit 40, the banks 53 and 54 function as the top boot type. If the address is made to appear in the order as shown by arrows 57 and 58, the banks 53 and 54 function as the bottom boot type.

[0044]

Conversion of the sector address in the case of Fig.5B is described below with reference to Figs.6A and 6B.

[0045]

The memory device shown in Fig.6A has a memory space of 8Mb, for example. The device has two boot blocks 59, each occupying 64Kb (=8Kb x 8) and defined as constituting a sector. The device also has 14 uniform sectors 60, each occupying a capacity of 64Kb.

[0046]

Therefore, the memory device in the drawing has a total of 16 sectors, each having a 64Kb capacity. Here, the address given in Fig.6A represents a physical address. Since there are 16 sectors, a sector address can be expressed by 4 bits.

[0047]

The present embodiment expresses a sector address by 4 bits of 16th through 19th bits of the address (here, referred to as A16 through A19 for convenience). Moreover, as to the external address, an E is prefixed to be referred to as EA16 through EA19, and an I is prefixed instead to the internal address to be referred to as IA16 through IA19.

[0048]

According to this notation, the sector-address conversion circuit 40 is a circuit that converts the external addresses EA16 through EA19 into the internal addresses IA16 through IA19, as shown in Fig.6B. The conversion may be performed with reference to a table as shown in Figs.7A, 7Band 7C or by circuits as shown in Figs.8A and 8B and Fig. 9.

[0049]

Figs.7A, 7B and 7C show translation tables for the address conversion using a conversion table. Fig. 7C is the translation table, and Fig. 7A and Fig.7B are a summary thereof for the top boot type and the bottom boot type, respectively. Here, a signal "#" used in Fig. 7A and Fig. 7B indicates an inverse. For example, "EA19" represents an inverse of "EA19", that is, if "EA19" is "1", "#EA19" is "0".

[0050]

If a sector address is set up like 55 and 56 in Fig.5B, the banks 53 and 54 will function as the top boot type, and if the sector address is set up like 57 and 58, the banks 53 and 54 will function as the bottom boot type.

[0051]

In addition, in the present embodiment, the external sector address bits EA16, EA17, EA18, and EA19 express 16 addresses from 0000 (reference number 66) to 1111 (reference number 67). All addresses 61 belong to the bank 53, and their EA19 that is the most significant bit of the address are "0". All addresses 62 belong to the bank 54, and their EA19 are "1". Therefore, the address bit EA19 identifies a corresponding bank.

[0052]

That is, when the EA19 is "0", an address belongs to the bank 53, and when the EA19 is "1", the address belongs to the bank 54.

[0053]

As mentioned above, the bank 53 is of the bottom

boot type. If the bottom boot type is desired, the internal address shall be the same as the external address. However, if the top boot type is desired for operation of the bank 53, the sector address is set up like 56 in Fig.5B. The set up is realized by making the internal address bits IA16, IA17, and IA18 (63) to take an inverse value of the address bits of EA16, EA17, and EA18, respectively.

[0054]

Similarly, since the bank 54 is the top boot type, the same setup as the external address shall be applied if the top boot type is desired. However, in order to operate the bank 54 as the bottom boot type, the sector address is set up like 57 in Fig.5B. To realize this, the internal address bits IA16, IA17, and IA18 (64) should be converted to an inverse value of the address bits of EA16, EA17, and EA18, respectively.

[0055]

The above describes how the tables of Fig.7A, Fig.7B and Fig.7C are prepared and used.

[0056]

Fig.8A is an embodiment example of the conversion circuit shown in Figs.6A and 6B.

[0057]

The conversion circuit includes a sector-address input terminal, a sector-address output terminal, a boot block type specifying terminal that specifies the boot block type of the memory device, and a signal conversion circuit. The conversion circuit converts a sector address impressed to the sector-address input terminal, based on the most

significant bit of the sector address and a signal impressed to the boot block type specifying terminal such that the memory device that contains the sector operates as a desired boot block type.

[0058]

The circuit of Fig.8A includes NOT circuits 70 and 71, AND circuits 72 and 73, an OR circuit 74, XOR circuits 75, 76, and 77, sector-address input terminals 100-103, sector-address output terminals 110-113, and boot block type specifying terminals 104 and 105 (a top boot type specifying signal input terminal and a bottom boot type specifying signal input terminal, respectively) that determine the boot block type of the memory device.

[0059]

This circuit converts the external address bits EA16, EA17, EA18, and EA19 to the internal address bits IA16, IA17, IA18, and IA19, respectively, as described above in reference with the tables in Figs.7A, 7B and 7C.

[0060]

As shown in Fig.8B, the bottom signal is put to "H" when the bottom boot type is desired, and the top signal is put to "H" when the top boot type is desired. It is inhibited that both the bottom signal and the top signal are put to "H" simultaneously.

[0061]

In the above, operation of the sector-address conversion circuit in Fig.8A has been described, where the bottom signal and the top signal are inputted from an external terminal.

[0062]

Fig.9 shows another example of the sector-address conversion circuit. In this example, sector addresses are converted by inputting a specified command into a control circuit of the memory device.

[0063]

The conversion circuit described in Fig.9 includes an address buffer 80 to store an address signal temporarily, an address pattern decoder 81 to decode a pattern of the address and obtain a timing signal, a control circuit 82 to control according to an inputted control signal, a command, and the like, a timing control circuit 83 to adjust timing of a latch circuit, a command decoder, and the like by acquiring timing from the output of the address pattern decoder 81, an input buffer 84 to store an incoming signal temporarily, a latch circuit 85 to latch input data, and a command decoder 86 to decode a command.

[0064]

The command decoder 86 outputs a sector-address conversion signal, based on the address signal, CE (Chip Enable), OE (Output Enable), WE (Write Enable) , and data (DQ).

[0065]

Fig.10 shows an example of a flash memory and its control circuit, which include a column gating (Y-gating) circuit 88 to open and close an input and an output of a column signal according to an output of a column address decoder (Y-decoder) 96, a cell matrix 89 which is a flash memory, a state control and command register 90 to temporarily store

a command and to control according to an input signal, a command and the like, an erase voltage generator 91 to generate the erase voltage for the flash memory, a writing voltage generator 92 to generate the writing voltage for the flash memory, a timer 93, a CE-OE logic circuit 94 to generate a control signal according to the CE signal and the OE signal received, an address latch 95 to latch the inputted address signal, the column address decoder (Y-decoder) 96 to decode a column address, a line address decoder 97 to decode a line address, an input/output buffer 98 to temporarily store input/output data, and a data latch circuit 99 to temporarily latch the data.

[0066]

In this configuration, the sector addresses are switched for a top boot type or a bottom boot type operation, by inputting data "AAH" to an address "AAAH" in the first bus cycle, inputting data "55H" to an address "555H" in the second bus cycle, and inputting data "2FH" to the address "AAAH" in the 3rd bus cycle in the case of a byte mode, as shown in a command list of Fig. 11.

[0067]

Next, a description will follow concerning a usage of the semiconductor memory device (also applicable to a semiconductor memory device functioning as two banks of the same boot block type using an address-conversion circuit) which has two banks (bank A and bank B) with the same boot block type, having a small sector at the most significant or the least significant physical address of each bank in reference with Fig.12.

[0068]

First, a rewriting program is loaded to the small sector of the bank A (S11), then, the uniform sector of the bank B is rewritten using this program (S12).

[0069]

Subsequently, the process jumps to the bank B (S13) to load the rewiring program to the small sector of the bank B (S15), and the uniform sector of the bank A is rewritten using this program (S16).

[0070]

In this manner, new data can be rewritten easily while data is maintained in the memory currently used within a system.

[0071]

[Advantages of the Invention]

According to the present invention, rewriting of a memory device is facilitated, and a memory device that operates as a desired boot block type irrespective of the original boot block type of the device becomes available.

[0072]

Further, when a plurality of small sectors are present in a memory device, a plurality of memory units with the top boot block or the bottom boot block become available, by providing an address-conversion circuit that defines an area of the boot block in the highest or in the lowest area of the sector address of the memory device. A system that conventionally had to use two or more memory devices can now be built by one memory device.

[0073]

Further, a system such as an STB and the like has conventionally been installed with two or more memory devices so that new data can be written to a memory, while maintaining data to a memory currently used, by storing the rewriting program in each boot block to rewrite data of the other memory alternately. Now, one memory device can provide the equivalent memory configuration.

[Brief Description of the Drawings]

Figs.1A and 1B are illustrative drawings showing a conventional memory device of a top boot type and a bottom boot type, respectively;

Fig.2 is a drawing showing rewriting of a memory device in an STB;

Fig.3 is a drawing showing a memory device that has two small sectors, one at the least significant sector address, and the other at the most significant sector address;

Figs.4A, 4B and 4C are drawings showing the principle of first sector-address conversion;

Figs.5A, 5B and 5C are drawings showing the principle of second sector-address conversion;

Figs.6A and 6B are drawings showing an example of sector-address conversion;

Figs.7A, 7B and 7C are drawings showing an example of a sector-address translation table;

Figs.8A and 8B are first drawings showing an example of a sector-address conversion circuit;

Fig.9 is a second drawing showing an example of the sector-address conversion circuit;

Fig.10 is a drawing showing a flash memory device and its control circuit;

Fig.11 is a drawing showing a command and address conversion of a flash memory; and

Fig.12 is a drawing showing an example of an operation method of a semiconductor memory device.

[Description of the Reference Numerals]
11, 16, 21, 26, 31, 32, and 43: Small Sector
10, 15, 20, 25, and 30: Memory Device
28, 70, and 71: NOT Circuit
40: Sector-Address Conversion Circuit
41: Address Decoder Circuit
42: Uniform Sector
48 through 54: Bank
59: Boot Block
60: Uniform Sector
72 and 73: AND Circuit
74: OR Circuit
75, 76, and 77: XOR Circuit
80: Address Buffer
81: Address Pattern Decoder
82: Control Circuit
83: Timing Control Circuit
84: Input Buffer
85: Latch Circuit
86: Command Decoder
88: Column Gating Circuit
89: Cell Matrix (Flash Memory)
90: State Control and Command Register
91: Erase Voltage Generator
92: Writing Voltage Generator
93: Timer
94: CE-OE Logic Circuit
95: Address Latch
96: Column Address Decoder
97: Line Address Decoder

98: Input/Output Buffer

99: Data Latch Circuit

100 through 103: Sector-Address Input Terminal

104: Top Boot Type Specifying Signal Input Terminal

105: Bottom Boot Type Specifying Signal Input Terminal

110 through 113: Sector-Address Output Terminal

~~【書類名】~~　~~図面~~　Name of the Document Drawing

~~【図１】~~

Illustrative Drawings Showing a Conventional Memory Device of a Top Boot Type and a Bottom Boot Type, Respectively

~~従来のトップ・ブート・タイプ及びボトム・ブート・タイプのメモリデバイスを説明するための図~~

~~FIG.1A~~

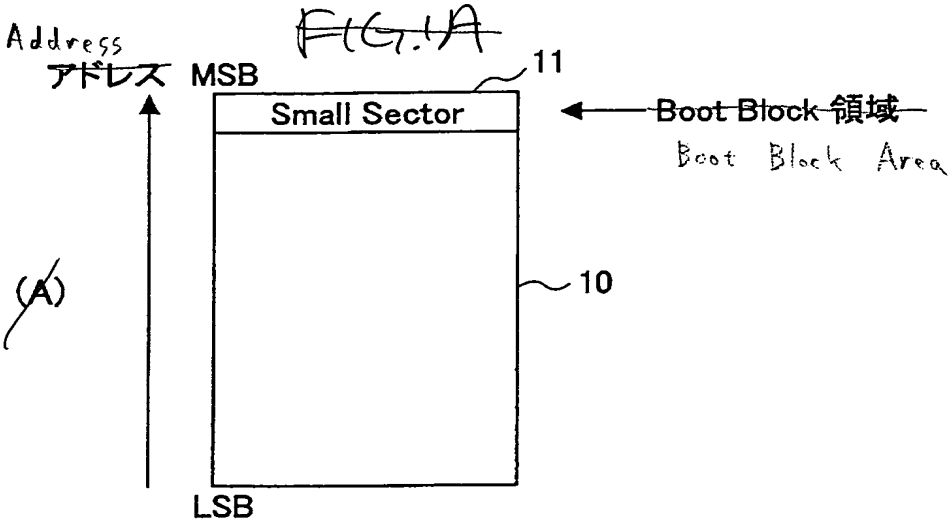


Fig.1A (A)

~~FIG.1B~~

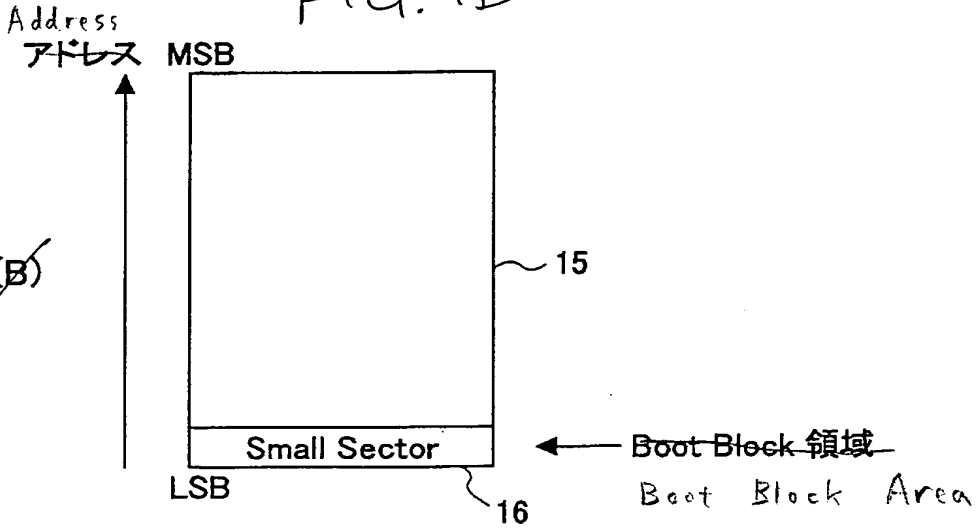
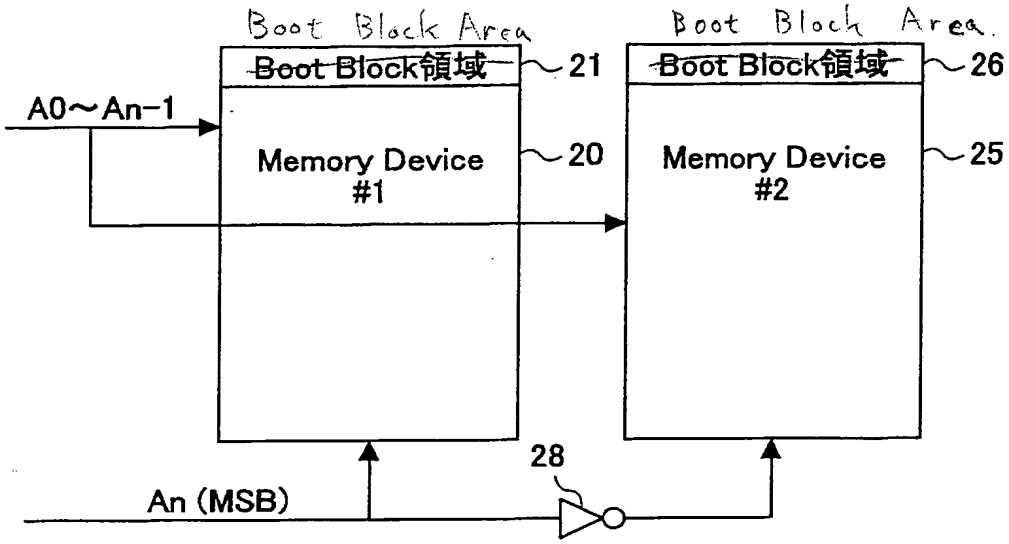


Fig.1B (B)

【図２】

FIG. 2

ＳＴＢにおけるメモリデバイスの書き換えを説明するための図　Drawing Showing Rewriting of a Memory Device in an STB

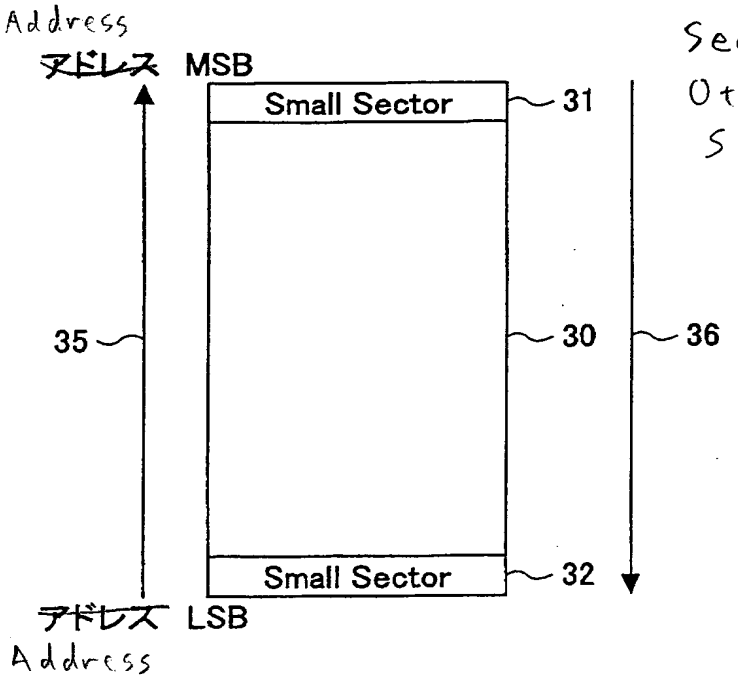


【図３】

FIG. 3

~~最下位のセクタアドレスと最上位のセクタアドレスにスモールセクタを有するメモリデバイスを説明するための図~~

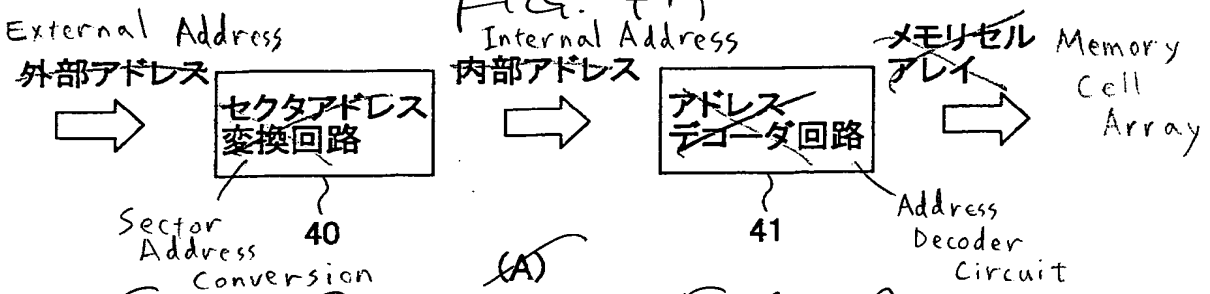
Drawing Showing a Memory Device that Has Two Small Sectors, One at the Least Significant Sector Address, and the Other at the Most Significant Sector Address



【図４】 Drawings Showing the Principle of First Sector-Address Conversion

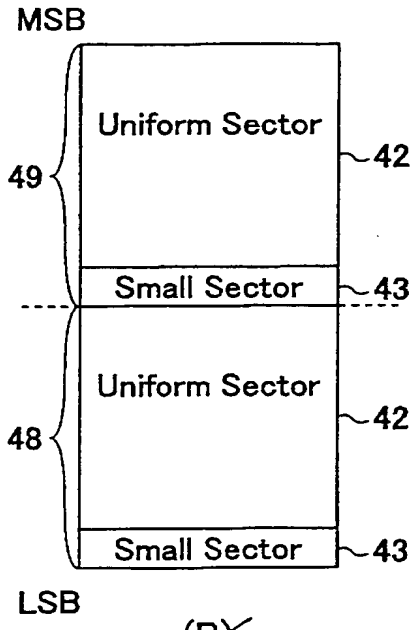
~~セクタアドレス変換の原理を説明するための図（その１）~~

FIG. 4A



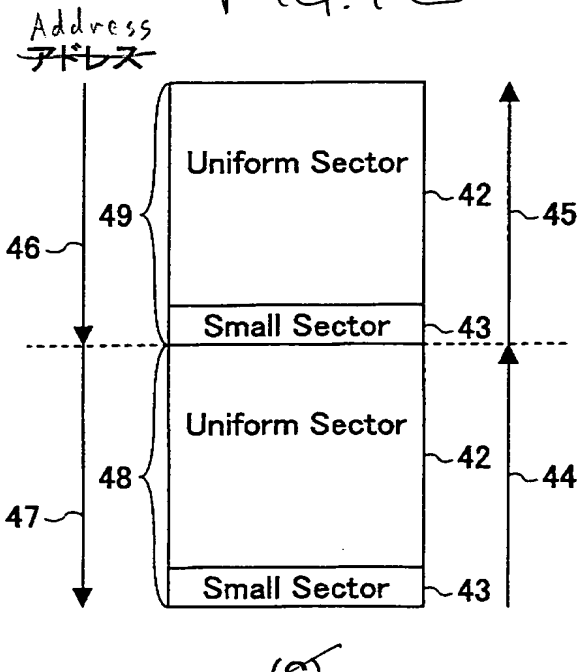
(A)

FIG. 4B



(B)

FIG. 4C



(C)

【図５】 Drawings Showing the Principle of Second Sector-Address Conversion

~~セクタアドレス変換の原理を説明するための図（その２）~~

FIG. 5A

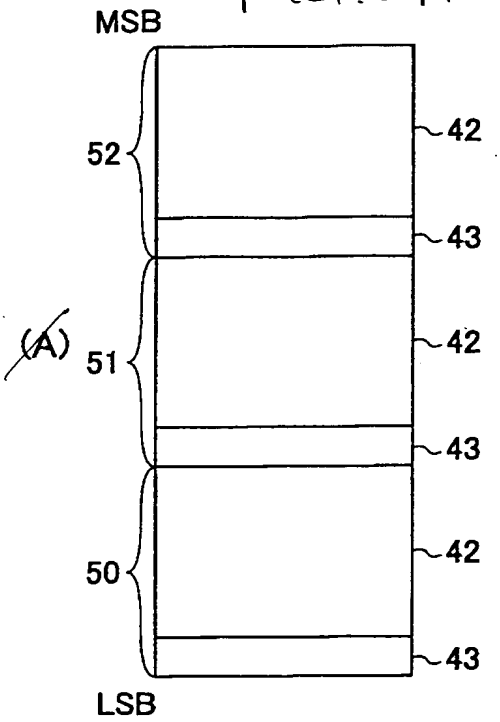


FIG. 5C

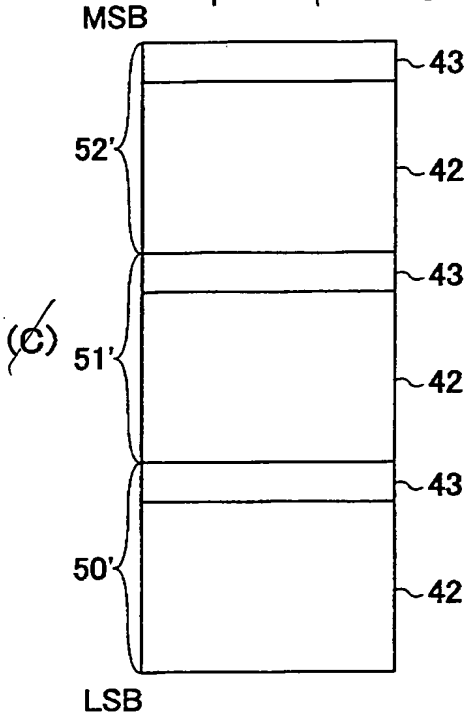
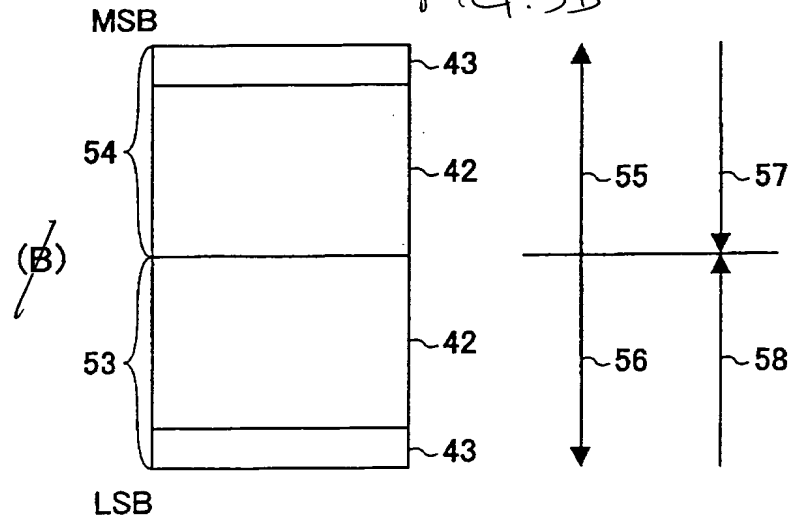


FIG. 5B



【図６】　Drawings Showing an Example of Sector-Address Conversion

~~セクタアドレス変換の例を説明するための図~~

FIG. 6A

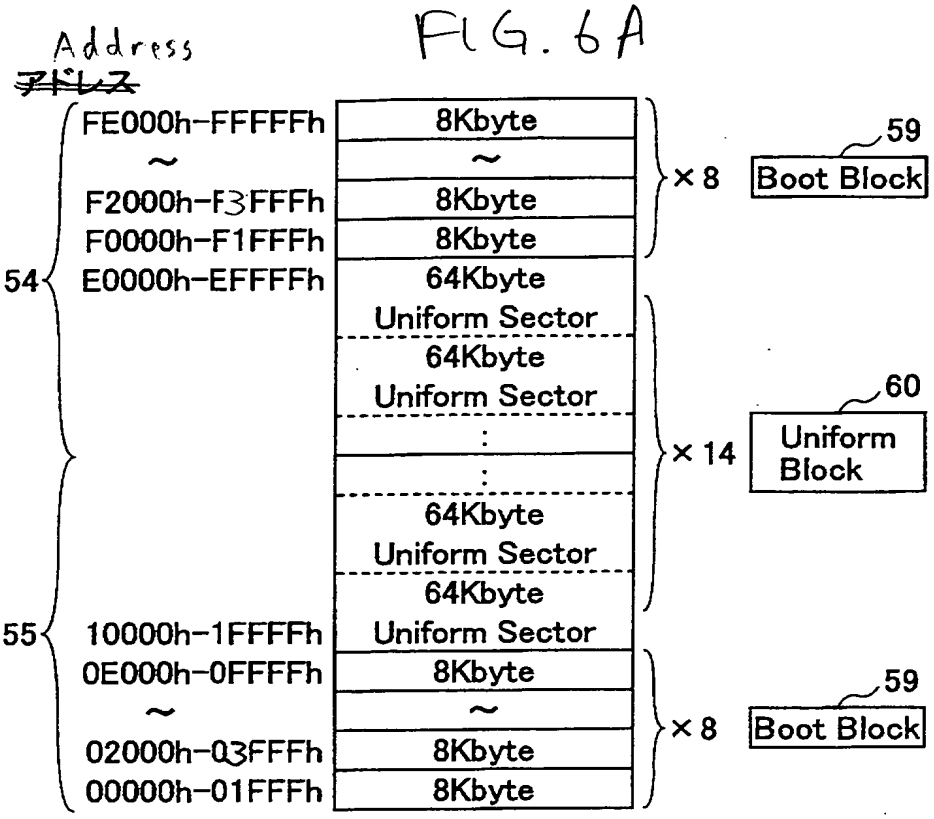
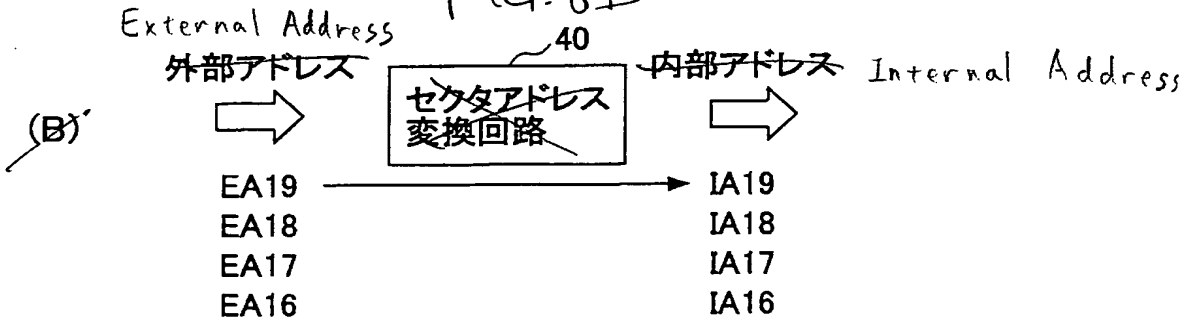


FIG. 6B



【図7】 Drawings Showing an Example of a Sector-Address Translation Table

~~セクタアドレス変換テーブルの例を説明するための図~~

FIG.7A(A)

~~Top Boot Typeへの変換テーブル例~~ Example Of Conversion Table For Top Boot Type

EA19	IA19	IA18	IA17	IA16
0	0	EA18#	EA17#	EA16#
1	1	EA18	EA17	EA16

FIG.7B (B)

~~Bottom Boot Typeへの変換テーブル例~~ Example Of Conversion Table For Bottom Boot Type

EA19	IA19	IA18	IA17	IA16
0	0	EA18	EA17	EA16
1	1	EA18#	EA17#	EA16#

FIG.7C (C)

	Top Boot Type				Bottom Boot Type			
	EA				IA				IA			
	19	18	17	16	19	18	17	16	19	18	17	16
66	0	0	0	0	0	1	1	1	0	0	0	0
	0	0	0	1	0	1	1	0	0	0	0	1
	0	0	1	0	0	1	0	1	0	0	1	0
	0	0	1	1	0	1	0	0	0	0	1	1
61	0	1	0	0	0	0	1	1	0	1	0	0
(~~バンク53に対応~~)	0	1	0	1	0	0	1	0	0	1	0	1
(Corresponds	0	1	1	0	0	0	0	1	0	1	1	0
To Bank 53)	0	1	1	1	0	0	0	0	0	1	1	1
	1	0	0	0	1	0	0	0	1	1	1	1
	1	0	0	1	1	0	0	1	1	1	1	0
	1	0	1	0	1	0	1	0	1	1	0	1
	1	0	1	1	1	0	1	1	1	1	0	0
62	1	1	0	0	1	1	0	0	1	0	1	1
(~~バンク54に対応~~)	1	1	0	1	1	1	0	1	1	0	1	0
(	1	1	1	0	1	1	1	0	1	0	0	1
67	1	1	1	1	1	1	1	1	1	0	0	0

63

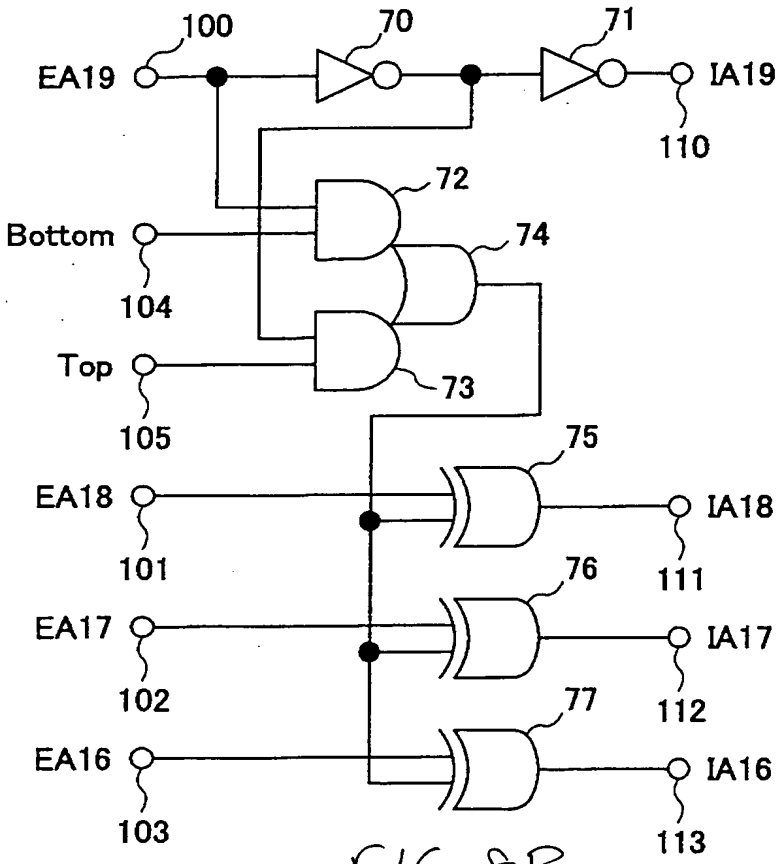
64

(Corresponds To Bank 54)

【図8】 First Drawings Showing an Example of a Sector-Address Conversion Circuit

~~セクタアドレス変換回路の例を説明するための図（その1）~~

FIG. 8A



(A)

FIG. 8B

(B)

~~Top入力端子~~	~~Bottom入力端子~~	~~アドレス変換後~~
0	0	~~どちらでもない（従来の方式）~~
0	1	~~Bottom選択~~
1	0	~~Top選択~~
1	1	~~禁止入力~~

Top Input Terminal

After Address Conversion

Neither (Conversion Method)

Selecting Bottom

Bottom Input Terminal

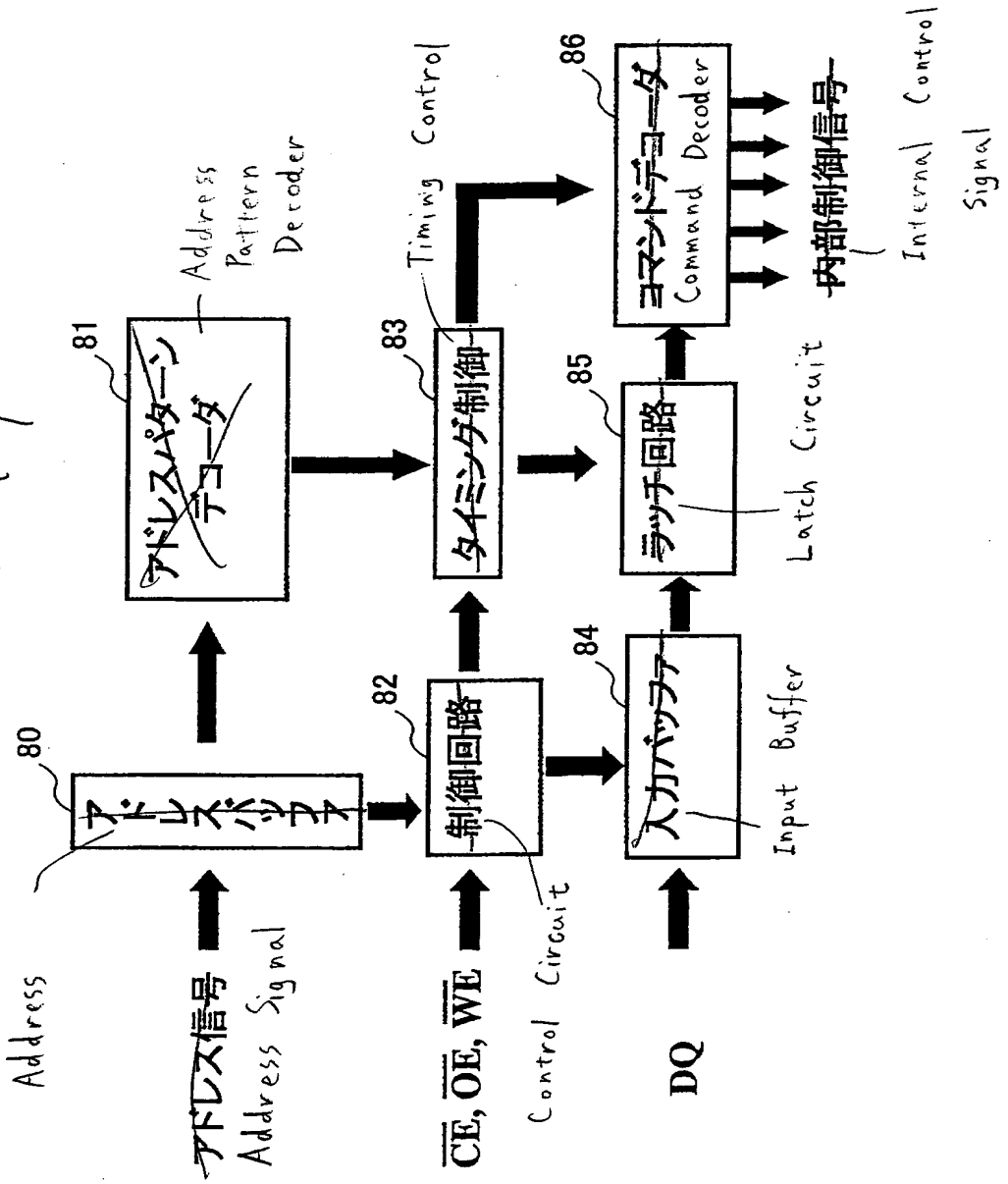
Input Inhibited

Selecting Top

【図９】　Second Drawing Showing an Example of the Second-Address Conversion Circuit

~~セクタアドレス変換回路の例を説明するための図~~
（その２）

FIG. 9



【図１０】 Drawing Showing a Flash Memory Device and its Control Circuit

~~フラッシュメモリデバイスとその制御回路を~~
説明するための図

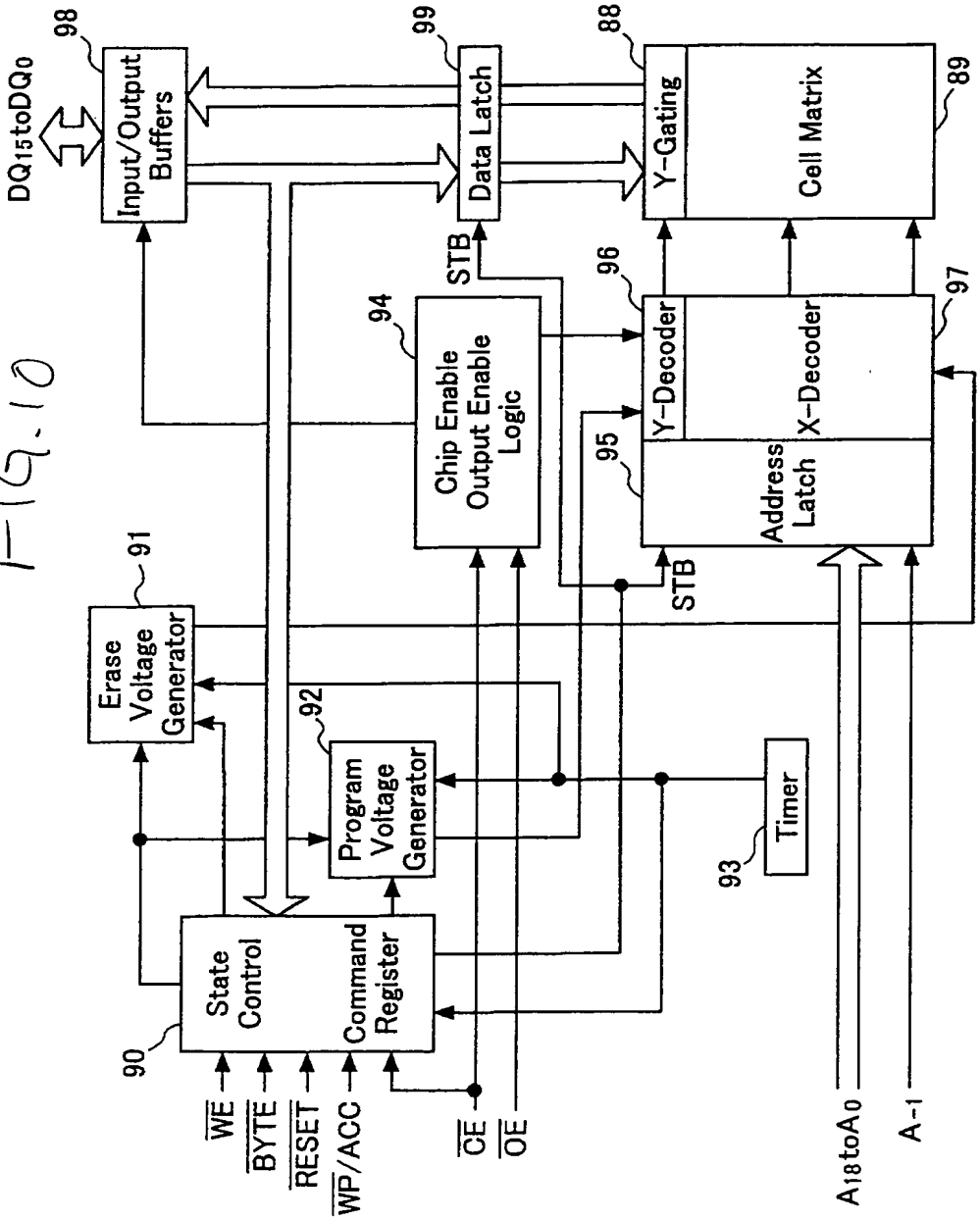


FIG. 10

【図１１】

Drawing Showing a Command and Address Conversion of a Flash Memory

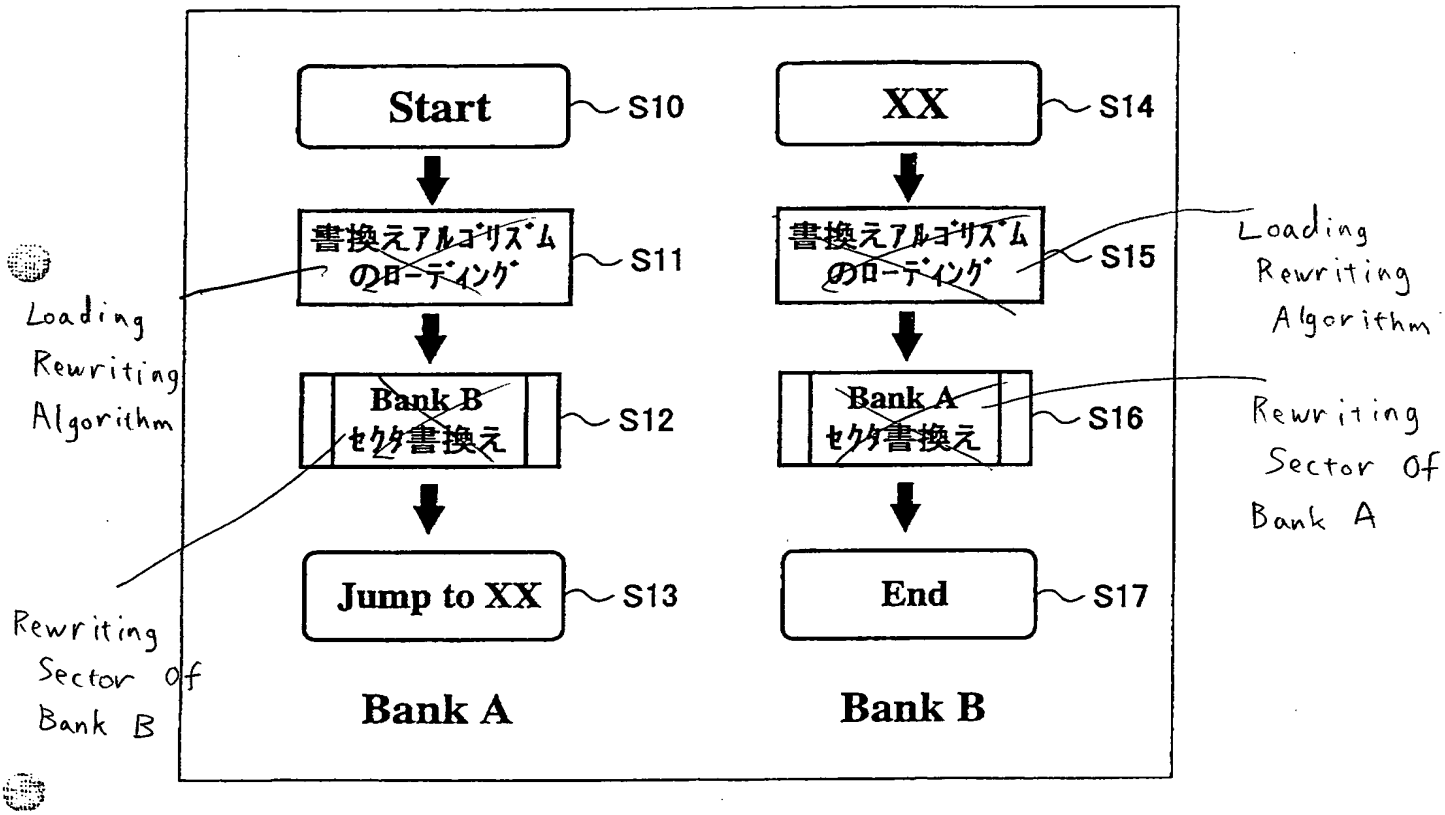
~~フラッシュメモリのコマンドとアドレス変換を説明するための図~~

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	Word /Byte	1	XXXH	F0H										
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD				
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	555H	90H						
	Byte		AAAH		555H		AAAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
	Byte		AAAH		555H		AAAH							
Chip Erace	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Sector Erace Suspend	Word /Byte	1	XXXH	B0H										
Sector Erace Resume	Word /Byte	1	XXXH	30H										
Set to Boot Sector	Word	3	555H	AAH	2AAH	55H	555H	2FH						
	Byte		AAAH		555H		AAAH							

FIG. 11

【図１２】 Drawing Showing an Example of an Operation Method of a Semiconductor ~~半導体記憶装置の利用方法の例を説明するための図~~ Memory Device

FIG. 12



[Name of the Document] Abstract

[Abstract]

[Object]

The present invention aims at providing a semiconductor memory device that can be operational in a desired boot block mode, regardless of the original boot block type of the device, by facilitating rewriting of the memory device.

[Solution Means]

(A) A sector address from an outside source is inputted into a sector-address conversion circuit 40, which converts the sector address into an internal address, and a memory cell array is accessed through an address decoder circuit 41. (B) Suppose that each of banks 48 and 49 of the memory device is configured as a bottom boot type. (C) By converting the sector address by the sector-address conversion circuit 40 such that the sector-address now appears to the outside in the reverse order as shown by arrows 46 and 47, each of the banks 48 and 49 now functions as a top boot type.

[Selected Figure] FIGs. 4A through 4C